Page 13, second full paragraph now reads as follows:

A2

When the power supply voltage VDDL is stabilized at time Td, the power-on detection signal /PORL attains the "H" level and the output signal from the inverter 12h responsively attains the "H" level of the power supply voltage VDDL. Responsively, the MOS transistors 12i and 12j are both turned on to discharge the node 12n to the ground voltage level, so that the main power-on detection signal /POROH from the inverter 12k attains the "H" level. Thus, when both of the power supply voltages VDDL and VDDH attain the stable state, the main power-on detection signal /POROH enters the "H" level inactive state.

Page 22, third full paragraph now reads as follows:

A3

The bit line precharge/equalization control circuit 22, the bit line isolation control circuit 23, the sense amplifier control circuit 24, the main word line drive circuit 20 and the sub-decoder 21 have the same structures as those of the level conversion circuit illustrated in Fig. 6 and each receives the high voltage VPP, or the DRAM power supply voltage VDDH or the array power supply voltage VDDS according to the amplitude of its output signal. To the main word line drive circuit 20, the sub-decoder 21, the bit line precharge/equalization control circuit 22, the bit line isolation control circuit 23 and the sense amplifier control circuit 24, the main power-on detection signal /POROH is applied. Also the write drive circuit WDR, the main power-on detection signal /POROH is applied. Also to the write drive circuit WDR,

Concld A3

the main power-on detection signal /POROH is applied.

Page 26, second full paragraph now reads as follows:

A4

At time T11, the logic power supply voltage VDDL is applied to have its voltage level increased. When at time T12, the logic power supply voltage VDDL is stabilized, the main power-on detection signal /POROH attains the "H" level and the converted voltage application detection signal /POROP responsively attains the "H" level as well (boosted voltage VPP level).

Page 31, first full paragraph now reads as follows:

A5

Fig. 14 is a diagram schematically showing a structure of a power-on detection signal generation unit according to the third embodiment of the present invention. In Fig. 14, the power-on detection signal generation unit includes: a power-on detection circuit 40 for detecting application of the logic power supply voltage VDDL to generate a logic power-on detection signal /PORL; a boosting circuit 42 for generating the boosted voltage VPP from the DRAM power supply voltage VDDH; a high voltage application detection circuit 44 for generating a high voltage application detection signal /PORP according to the voltage level of the boosted voltage VPP from the boosting circuit 42; and a main power-on detection circuit 46 for generating a main power-on detection signal /POROP which is rendered inactive when both of the logic power-on detection signal /PORL and the high voltage application detection signal /PORP are inactivated.